Enhancing Semiconductor Test Efficiency: The Johnstech J-Tuning Process

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Introduction:

The semiconductor industry operates within a dynamic landscape, characterized by ever-evolving technologies and demanding performance requirements. Semiconductor test engineers play a critical role in ensuring the accuracy and reliability of testing processes, ultimately influencing the quality and success of semiconductor devices. To ensure maximum electrical performance, Johnstech International Corporation has developed the J-Tuning process—a systematic approach to optimizing test socket designs. In this white paper, we explore the J-Tuning process and its impact on enhancing semiconductor test efficiency.

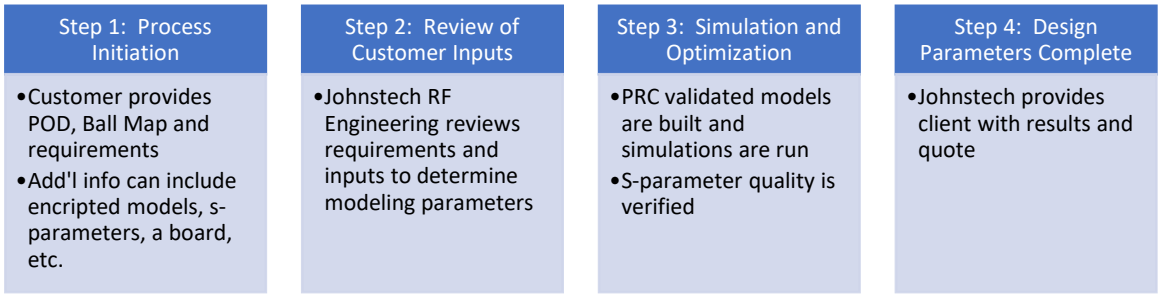

Figure 1: Shows the steps of the J-Tuning process.

Process Initiation:

The J-Tuning process commences with a pivotal phase centered around gathering comprehensive input from the customer. This input typically includes critical documents such as Package Outline Drawing (POD), Ball Map, and specific requirements tailored to the customer's testing needs. These requirements may encompass a wide array of technical details, ranging from encrypted models and S-parameters to load board layouts and thermal considerations.

By soliciting these essential documents and requirements, Johnstech's engineering team gains invaluable insights into the intricacies of the customer's testing environment and objectives. Johnstech provides test solutions that guarantee mechanical and electrical contact with the DUT and loadboard. The ball map will inform Johnstech of the RF signal configuration and number of grounds. This information along with S-parameters of the DUT are essential to inform optimal inductance of the test socket based on inductance sensitivity of the DUT. The collaborative exchange of information lays the groundwork for a tailored approach, ensuring that the subsequent phases of the J-Tuning process are finely attuned to the customer's unique requirements and provide the most cost-effective solution.

Review of Customer Inputs:

Johnstech engineering reviews all customer inputs and testing requirements, clarifying any information or understanding as needed. The team conducts a detailed analysis to identify if standard test contactor solutions meet the customer needs or if custom J-Tuning is required. Standard designs make use of identical contactors throughout, to simplify test contactor maintenance over the life of the product. However, J-Tuning may require mix and match design, potentially using contacts / probes of multiple pitches within the same test contactor. For this reason, Johnstech International has device families for solid contacts and spring pins in which different thickness contacts or pitch of pins share a common test height. This phase concludes when all inputs necessary for successful simulation have been identified and provided.

Simulation and Optimization:

In this phase, Johnstech's engineering team harnesses advanced simulation techniques, particularly utilizing HFSS simulation methods tailored for RF modeling. HFSS, a high-frequency electromagnetic simulation tool, enables precise modeling and analysis of complex RF structures, ensuring accurate representation of the test socket's electrical behavior at the desired frequency range.

Employing HFSS methodology, Johnstech engineers conduct in-depth simulations to refine design parameters and optimize performance characteristics. By adjusting contactor geometry, contactor bandwidths, and impedance matching configurations, Johnstech's objective is to achieve optimal signal integrity and impedance characteristics tailored to the customer's specific requirements.

Throughout this collaborative process, Johnstech actively engages with the customer to ensure alignment with their objectives and preferences. This iterative approach allows Johnstech to explore various design alternatives and deliver customized solutions that effectively address the customer's unique testing challenges. This phase concludes with a customer-approved solution that demonstrates optimal simulated results.

Design Parameters Complete:

Upon completion of the simulation and optimization phase, the finalized design parameters are documented and validated. Johnstech's engineering team then translates the results from simulation into the actual final design concept. The final design concept is then sent to the client for review and approval. The resulting test socket design represents a tailored solution optimized for the specific needs and requirements of the customer.

Case Study Example 1 – High Frequency:

In this example, the customer required a test socket solution that offered enhanced Insertion Loss and Return Loss in a GSG configuration. The J-Tuning Process Initiation commenced and gathered customer inputs. In this case, a standard solution using all 0.5mm (native pitch) pins was compared with a J-Tuned custom option of mixed pitches that utilized a standard test height. The J-Tuned solution enhanced performance for this particular application by providing an impedance match closer to the 50 ohm target for this solution.

The simulated results in Insertion Loss are shown in Figure 2. Johnstech was able to baseline a SHOTO 0.5mm pitch design that initially showed an Insertion Loss of -1.0 dB @ 8 GHz for this application.

However, the revised J-Tuned test socket showed an Insertion Loss of -1.0 dB @ 24 GHz. This represented a threefold performance gain.

The simulated results in Return Loss are shown in Figure 3. Johnstech was able to baseline a SHOTO 0.5mm pitch design that initially showed a Return Loss of -10 dB @ 7 GHz in the application. However, the revised J-Tuned test socket showed a Return Loss at -10 dB @ 26 GHz. Of note, the client also had an opportunity to revisit the Return Loss goal and selected a final performance of -20 dB @ 22 GHz. This final performance demonstrated a 3 times improvement in bandwidth with a specification 10 times better than the original target.

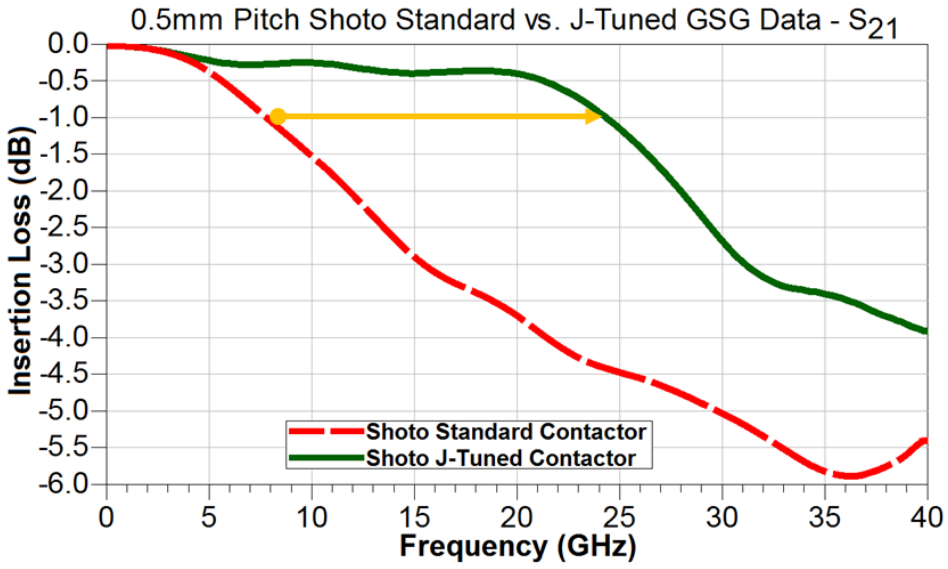

Figure 2: Example of J-Tuned solution Insertion Loss performance improvement for a GSG configuration.

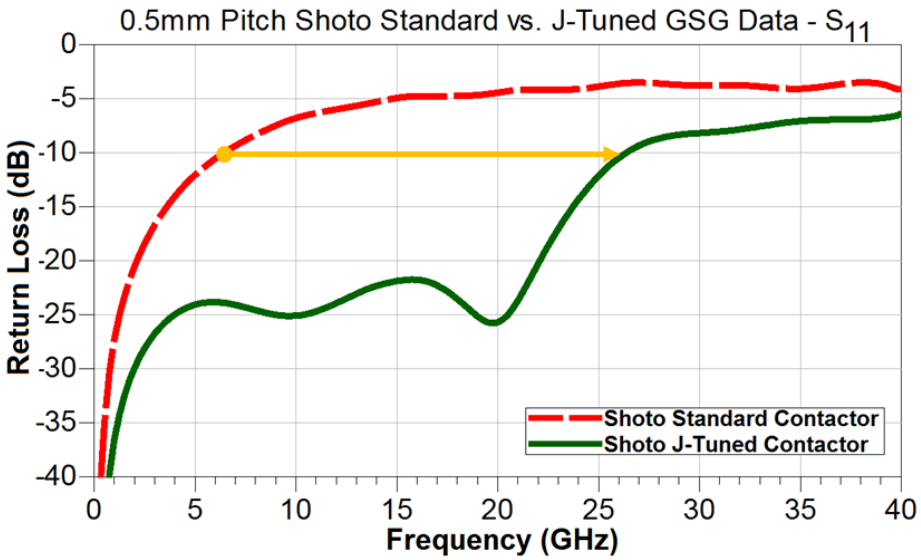

Figure 3: Example of J-Tuned solution Return Loss performance improvement for a GSG configuration.

Case Study Example 2 – High-speed Digital:

In this example, the customer had similar requirements to those in Example 1, but with a GSSG configuration. This particular customer DUT used a GSSG configuration to mitigate the amount of noise between signals in a high-speed digital application. Similar to the approach used in Example 1, the Example 2 customer could accommodate a design that mixed probe pitches to deliver outstanding impedance matching of the GSSG differential pair. When comparing the J-Tuned design to that of a standard SHOTO design in Figure 4, the custom J-Tuned solution shows a fourfold Insertion Loss upgrade from 9.5 GHz to over 40 GHz. The close impedance matching of the J-Tuned solution also delivered a Return Loss advancement at -10 dB from 15 GHz to 40 GHz as shown in Figure 5. In this digital application, this resulted in the contactor optimally supporting the third harmonic of 12 Gps digital signal.

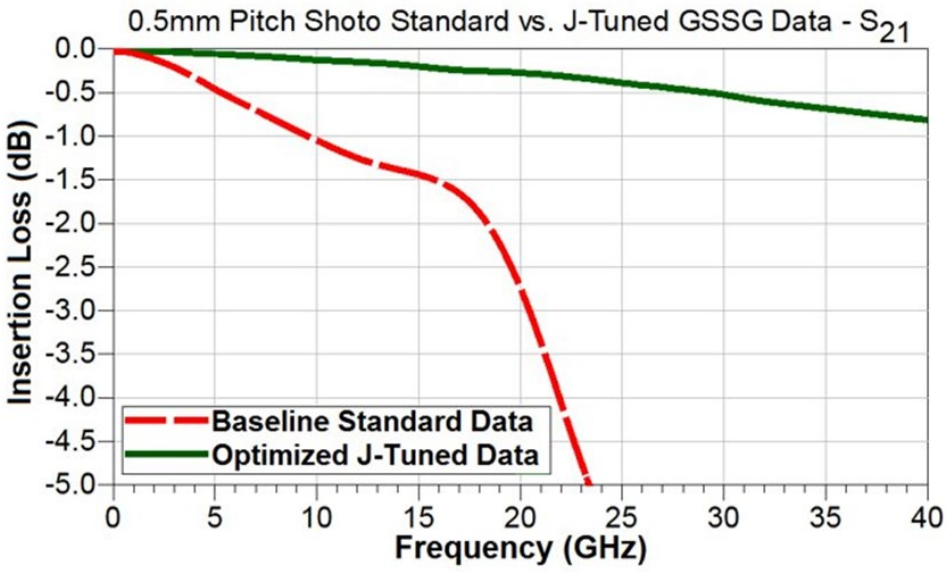

Figure 4: Example of J-Tuned solution Insertion Loss performance improvement for a GSSG configuration.

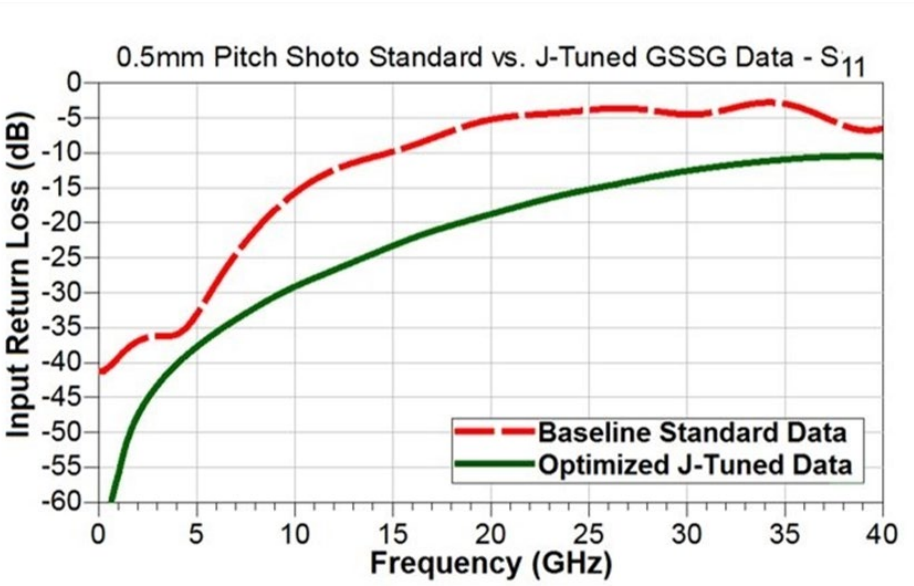

Figure 5: Example of J-Tuned solution Return Loss performance improvement for a GSSG configuration.

Case Study Example 3 – BAW Filter

In this example, the customer was interested in improving the performance of a 5G BAW filter with a GSG signal configuration. Because filters can be so sensitive to inductance, a Johnstech Performance Plus solution was identified wherein specific ground inserts were used to minimize inductance – in this case down to 0.003 nH from test socket to ground plane.

Figure 6 shows the filter performance under various scenarios. The device performance alone (when soldered) and the device in a contactor with theoretical inductance of 0 nH are shown to serve as benchmarks of maximum theoretical performance. This test socket solution utilized a Performance Plus design with ROL100A contacts and a metal housing. The contactor also featured a ground insert that lowered inductance in the initial design to 0.003 nH. Further J-Tuning added numerous additional ground contact connections yielding a final design inductance of 0.00003 nH. This final configuration with ultra-low inductance dramatically lowered the filter skirt to provide improved BAW filter testing performance to the customer, resulting in an increased test yield.

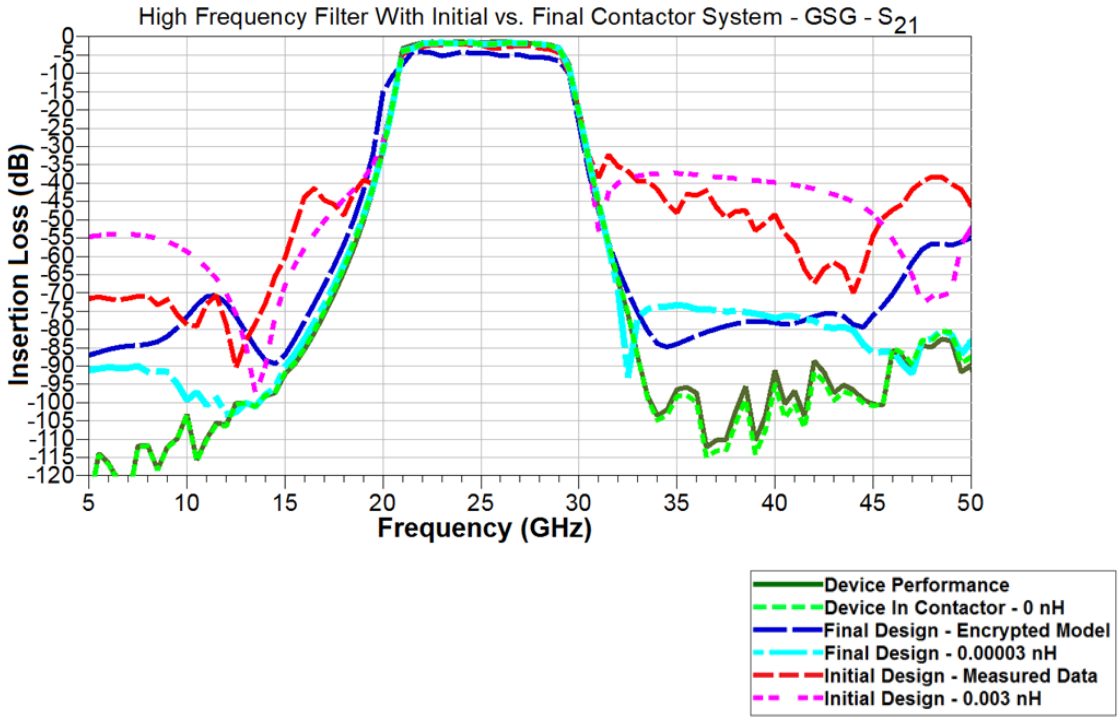

Figure 6: Highlights J-Tune (Final Design) device performance improvements in a BAW filter application with GSG signal configuration.

Case Study Example 4 – Addressing Mismatch Loss

In this example, the customer had a specific need to implement a test solution that provided ideal return loss and crosstalk to effectively reduce the mismatch loss during test. Mismatch loss is defined by the following equation:

Mismatch loss = $10 \log (S + 1)^2 / 4S$

Where the voltage standing wave ratio (VSWR) = $S = (1 + |\Gamma|) / (1 - |\Gamma|)$

Where $\Gamma = (Z_L – Z_o) / (Z_L + Z_o)$

The mismatch loss equation demonstrates the importance of matching the impedance as closely as possible to the desired value.

The J-Tuned process compared an initial design utilizing a standard VROL200 contactor to a J-Tuned VROL200 contactor with enhancements to match impedance as closely as possible to 50 ohms. Figure 7 shows the resulting insertion loss performance improvement for the J-Tuned solution. Insertion Loss at -1 dB advanced from 25 GHz to 53 GHz. Figure 8 shows the resulting return loss performance change. Note that the J-Tuned version shows a -40 dB return loss to 12 GHz, where the standard solution started with a -20 dB return loss to 7 GHz.

It is worth noting in Figures 7 & 8 that there is outstanding performance at and below 10 GHz for the J-Tuned VROL solution. Since the vast majority of semiconductor devices operate below 10 GHz, the J-

Tuned VROL200 would be an ideal solution for almost all Analog, Digital, and RF package types supported by VROL including QFN, DFN, and all manner of leaded products such as SOP, TSOP, and QFP.

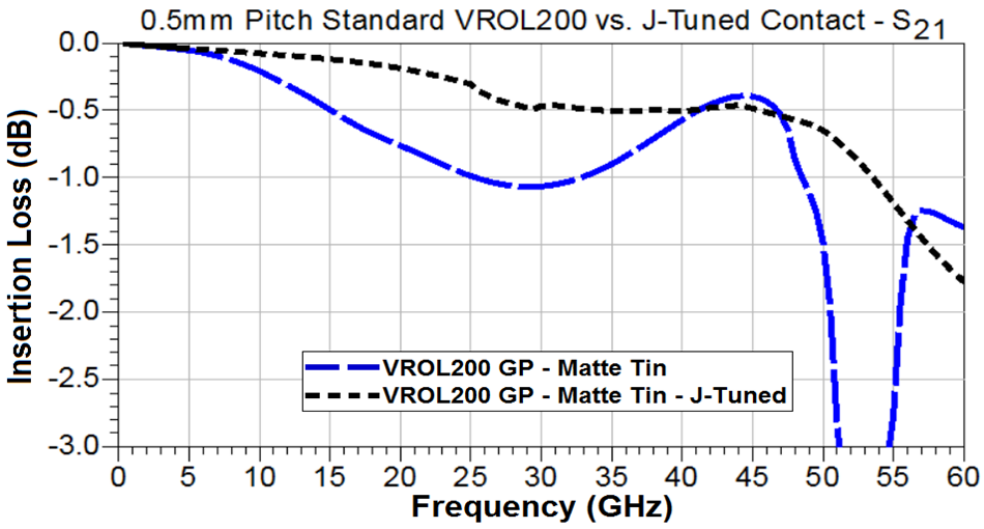

Figure 7: Shows the Insertion Loss improvement of a J-Tuned VROL solution.

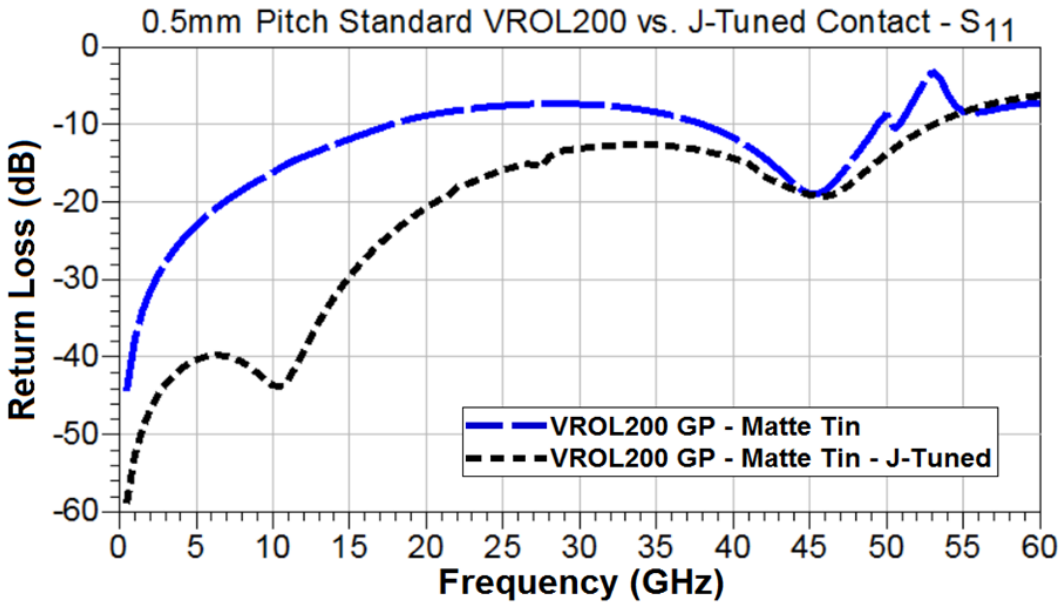

Figure 8: Shows the Return Loss improvement of a J-Tuned solution.

Conclusion:

The J-Tuning process represents a systematic and collaborative approach to optimizing test socket designs for semiconductor testing applications. By leveraging customer inputs, advanced simulation

techniques, and iterative optimization cycles, Johnstech delivers tailored solutions that address specific testing challenges and performance requirements. Through proactive collaboration and a commitment to excellence, Johnstech empowers semiconductor test engineers to achieve superior testing efficiency and reliability. As demonstrated in the numerous case study examples, Johnstech J-Tuned solutions can benefit a wide variety of applications. While this white paper focused more on improvements in Insertion Loss and Return Loss, Johnstech also partners with clients to overcome crosstalk and isolation challenges through J-Tuning.

For more information on the J-Tuning process and Johnstech's comprehensive range of test socket solutions, please visit Johnstech.com or contact our team of experts.

Website: https://www.Johnstech.com/

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